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Efficient Design of Truncation and Rounding Based Approximate Multiplier

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Abstract: The increasing complexity of the DSP systems demands higher computational performance in its architecture. But the traditional DSP arithmetic has limits in terms of speed of calculations. Moreover, in some applications, speed is more important than accuracy. To further enhance performance, approximate arithmetic circuits are designed with some loss of accuracy to reduce power consumption and increase speed. Furthermore, these approximate circuits have been considered for error-tolerant applications. In this paper, we propose a truncation and rounding-based approximate multiplier. In this multiplier, the operands are rounded to the nearest exponent of two and adder, and shifters are used at the final multiplication stage. This proposed multiplier simplifies multiplication operation, thus reducing area, power, and increasing speed. Simulation results reveal that the proposed approximate multiplier improves delay, area, and power consumption up to 9.3%, 37%, and 6.6%, respectively, compared to the ROBA multiplier. The proposed multiplier was synthesized and simulated using Xilinx Vivado 2016.4 environment.

Index Terms – Truncation, Rounding, Adders, Shifters, Approximate Computing, DSP.

I. INTRODUCTION

Electronics are continuously upgraded, particularly in digital signal processing and multimedia applications. Nowadays, they are growing day by day. In this DSP and Multimedia applications, it requires many arithmetic multiplications. Different types of multipliers perform these multiplication operations. Multipliers play a vital role in most high-performance systems. When considering digital signal processors and microprocessors, a multiplier is a crucial component for logical operation. In DSP methods, we utilize Fourier Transformations and discrete cosine transformations in DWT. Multiplication is more delayed and power-consuming as we evaluate other arithmetic operations. The main challenge in designing the multiplier is reducing the delay and minimizing the area with efficient power usage. To accomplish this test by decreasing the number of partial products. Even if the number of partial products is reduced by utilizing a higher radix booth encoder, the number of complex multipliers that are expensive to generate increases concurrently. By utilizing the Canonic Sign Digit representation (CSD), we can encode minimum non-zero digit coefficients [1]. Canonic Sign Digit multipliers give fewer non-zero unfinished products that diminish their switching action. In CSD, encoding additionally has different constraints. Folding technique that limits silicon zone by utilizing time-multiplexing action into single practical units, for instance, adders, multipliers is not conceivable as the Conic Sign Digit based multipliers are hard-wired to particular co-efficient.

CSD-based programmable multiplier arrangement was specially planned for social events of pre-chosen coefficients that give particular features. The degree of ROM is utilized to accumulate the get-together of coefficients. It diminishes the area and power usage of the circuit. In any case, this multiplier design is not versatile. Since the fractional items age unit is intended for a specific gathering of coefficients and can not be reutilized for different gatherings, also, this method is difficult to extend massive groups of predetermined coefficients accomplished simultaneously for high efficiency [2]-[7]. Modified Booth (MB) encoding solves the previously mentioned limitations and decries the count of the partial products to half. We can minimize the area with efficient power usage and delay by reducing the partial products. In [8], Kim et al. anticipated a procedure like laying out more capable MB multipliers for social affairs of pre-chosen coefficients with measure up to obstructions indicated in the before section. In [9]-[11], multipliers are incorporated in butterfly units of FFT processors utilize coefficients which standard to put away in ROMs.

Energy minimization is one of the main design requirements in almost any electronic system, especially portable ones such as smartphones, tablets, and different gadgets. Therefore, achieving this minimization with minimal performance (speed) penalty is highly desired. However, Digital signal processing (DSP) blocks the re-key components of these portable devices for realizing various multimedia applications. The computational core of these blocks is the arithmetic logic unit, where multiplications have the greatest share among all arithmetic operations performed in these DSP systems. Therefore, improving the speed and power/energy-efficiency characteristics of multipliers plays a key role in improving the efficiency of processors. Furthermore, many DSP cores implement image and video processing algorithms where final outputs are images or videos prepared for human consumption. This fact enables us to use approximations for improving speed/energy efficiency.